REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 12-17 and 23-36 remain pending. Claims 23-36 have been allowed. Claims 12-17 have been rejected.

Claims 12 and 17 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicant submits that the amendments do not add new matter.

ALLOWABLE SUBJECT MATTER

Applicants note with appreciation the Examiner's allowance of the claims 23-36.

REJECTIONS UNDER 35 U.S.C. § 103

Claims 12-17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,495,467 to Shin, et al. ("Shin"), in view of U.S. Patent No. 5,091,326 to Haskell ("Haskell"), further in view of U.S. Patent No. 6,197,639 to Lee et al. ("Lee").

Applicants have amended claim 12 to particularly point out that a bit line is formed in the slot to contact the active regions. The one-dimensional slot has a length along the length of the bit line. The length of the one-dimensional slot is substantially larger than a width. The width of the one-dimensional slot is the gate stack width.

The Examiner acknowledged that "Shin et al. fail to disclose the required slot/pattern in interlayer dielectric and the required bit lines" (Office Action, 03/27/06, p.2).

Shin discloses a memory device having the U-shaped floating gate to increase coupling between the floating gate and the control gate. More specifically, Shin discloses forming a floating gate F1' on tunnel oxide layer (101), patterning, and then etching the floating gate F1' to form a U-shaped floating gate F1'. The interlayer dielectric 109 is deposited on the floating gate

F1', and then control gate 110 is deposited on the interlayer dielectric 109 (Figures 1-10, col. 4, line13- col. 6, line 34).

Haskell, in contrast, discloses fabricating contacts for EPROM elements. More specifically, Haskell discloses forming a multilayer structure consisting of a field oxide 28a, etch stop layer 28b, oxide layer 28c, and polysilicon layer 28d on substrate 16. The multilayer is structure is etched according to a pattern defined by a slot mask that defines the interconnect areas (col. 5, lines 45-65).

Thus, Haskell, similarly to Shin, fails to disclose the one-dimensional formed in the ILD that has a length along the length of the bit line that is substantially larger than a width that is the gate stack width. Additionally, Haskell, similarly to Shin, fails to disclose a bit line formed in the slot to contact active regions, as recited in amended claim 12.

Lee, in contrast, discloses forming bit line contact regions independently from the word line contact regions. More specifically, Lee discloses forming a bit line contact region 85 by etching the ILD layer 81 (Figure 9, col. 4, lines 59-64), forming metal plug 97 in the bit line contact region 85 (Figure 11, col. 5, lines 47-50), forming ILD layer 99 having via holes on the ILD layer 81, and then forming metal layer patterns 100 in the via holes 98 (Figure 12, col. 5,lines 56-64).

Thus, Lee discloses forming metal layer patterns 100 in the via holes. In contrast, amended claim 12 refers to a bit line formed in the slot to contact the active regions, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width that is the gate stack width.

It is respectfully submitted that Shin does not teach or suggest a combination with Haskell and Lee, Haskell does not teach or suggest a combination with Shin and Lee, and Lee does not teach or suggest a combination with Shin and Haskell. Shin teaches a U-shaped floating gate to increase coupling to a control gate. Haskell teaches fabrication of contacts to EPROM

elements. Lee teaches forming the bit line contact regions of the cell array independently from the word line contact region to avoid over-etching. It would be impermissible hindsight based on Applicants' own disclosure, to combine Shin, Haskell, and Lee.

Furthermore, even if Shin, Haskell, and Lee were combined, such a combination would lack the following limitations of amended claim 12: a bit line formed in the slot to contact the active regions, wherein the one-dimensional slot has a length along the length of the bit line that is substantially larger than a width, that is the gate stack width.

Therefore, Applicants respectfully submit that amended claim 12 is not obvious under 35 U.S.C. § 103(a) over Shin, in view of Haskell, and further in view of Lee.

Because claims 13-17 depend from amended claim 12, and add additional limitations, Applicants respectfully submit that claims 13-17 are not obvious under 35 U.S.C. § 103(a) over Shin, in view of Haskell, and further in view of Lee.

CONCLUSION

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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Date: June 26, 2006 By: _____

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